Docket No. BU9-98-179

Remarks

Claims 1, 2, 4-7, 14, and 15 were rejected by the Examiner under 35 U.S.C. § 102(e) as being anticipated by Ono (U.S. Patent No. 5,966,606, hereinafter "Ono").

Applicants respectfully traverse the Examiner's rejection.

Per the Examiner,

"Ono discloses forming a polysilicon portion 23 of a gate conductor on a substrate 21 having a semiconductor portion, and forming a nitrided film 27 on the surface of the polysilicon portion. Trimming of the polysilicon portion would be obtained in such a process because the same materials are treated in the same manner. He discloses that the nitrided film comprises selective surface nitridation. He teaches as well, selectively compensating n-channel and p-channel devices, and at least partially removing the nitrided film. He also discloses anisotropically etching the nitrided film, forming gate conductor spacers, and forming an additional oxide layer on the nitrided film. (Figures 4A-4E, Column 3 lines 10-11, and 21-24, Column 4, lines 21-26, 32-41, 47-51, and 62-64, Column 5, lines 10-22, and Column 6, lines 26-31)."

Applicants respectfully disagree and submit that the claims are patentably distinct over the cited references. Specifically, Applicants submit that Ono fails to disclose "trimming" the gate as recited in independent claim 1 and similarly recited in independent claim 14.

Applicants respond further to the Examiner's rejection with an explanation and traverse. The purpose of gate trimming is to change the gate size and dimensions in order to change the gate's electronic performance. (Application, Page 2, lines 3-5). Gate trimming is accomplished by chemically reacting the portion of the gate to be trimmed away into a

nitride or oxide and then selectively etching that nitride away, leaving a gate of smaller, trimmed dimensions. (Application FIGS. 3 & 4). The portion of the silicon gate that is reacted is thereby removed (trimmed) as the etched-away nitride. Another approach is to leave the nitride in place, recognizing that the silicon portion of the gate is now reduced (trimmed) and coated with the insulating nitride. An important feature of the method is the depth of the chemical reaction into the polysilicon gate material, because this determines the amount of gate material trimmed. To avoid superficial films, pressurized gases and laser energy are used to heat and react the silicon to the desired depth. (Application, page 15, lines 9-19) Once a desired portion of the gate silicon has been reacted, the nitride can remain as an insulating layer or be selectively etched away, taking the reacted portions of the gate with it. The antithesis of trimming is superficial coating, where the amount of the gate silicon reacted is too small to significantly change the electronic properties of the gate.

Ono teaches away from gate trimming because he teaches only superficial coatings that are either too thin (2-4 nm) to impact the electronic properties of the gate (Ono, column 4, lines 21-35; column 5, lines 58-60) or which are chemical vapor depositions (CVDs) that carry their own silicon and thus do not react the gate silicon (Ono, column 4, line 62 to column 5, line 1). Ono does not achieve the same effect as Applicants because Ono is focused on avoiding changes to the gate's electronic properties and Applicants are focused on making changes to the gate's electronic properties. The whole thrust of Ono's invention is to prevent changes to the gate's electronic properties from those that existed when the gate was first formed. (Ono, column 3, lines 30-33). The object of Ono's invention is to prevent the formation of "bird beaks" in the gate insulator which degrade the electronic properties of the gate as formed. (Ono, column 2, lines 63-67) Ono never obtains trimming of the gate silicon.

Ono's oxide layer is a CVD layer supplying it own silicon and oxygen. It is not intended or alleged to chemically react with an electronically significant portion of the gate silicon. (Ono, column 4, line 62 to column 5, line 1).

Ono's nitride layer is made hot and fast so as not to effect the electrical properties of the transistor. (Ono, column 4, lines 21-33; column 5, lines 52-60). The pressure is ambient atmosphere (Ibid.), so chemical reaction at depth in the gate silicon is not accomplished.

Applicants' nitride layer is tens of nanometers thick (Application, page 15, lines 3-5) and trims an electrically significant portion of the gate, changing the performance of the transistor.

not recited

The other features which the Examiner cited specifically are, taken individually, away from the point of novelty of Applicants' invention and comprise practices in the art recited to complete the description of the method of making the invention as part of a chip (i.e., forming sidewalls, source, and drain regions).

In summary, Applicants' invention is not anticipated by Ono. Ono teaches away from Applicants' invention.

Claims 8-10 and 17 were rejected by the Examiner under 35 U.S.C. § 103(a) as being unpatentable over Ono (U.S. Patent No. 5,966,606, hereinafter "Ono") in view of Moslehi et al (U.S. Patent No. 4,715,937, hereinafter "Moslehi").

The Examiner stated that:

"Ono does not disclose forming the nitride film by the method of claims 8-10 and 17. Moslehi et al discloses laser enhanced nitridation of silicon to form a nitrided film (Column 2, lines 8-15). It would have been within the scope of one

of ordinary skill in the art to combine Ono and Moslehi et al to achieve the formation of nitride film 27 of Ono. The Examiner takes official notice that the use of NH_3 as the nitridizing gas was known at the time of applicant's invention. It would have been within the scope of one of ordinary skill in the art to use the known gas process to achieve the nitridizing step of the combination of Moslehi et al and Ono, in view of the recognized suitability of such a step."

The Applicants respectfully traverse the Examiner's rejection. Neither Ono nor Moslehi nor their combined efforts teach "trimming" as recited in independent claims 1 and 14 of the present Application.

Because Ono does not anticipate the Applicants' invention, as discussed above, the combination of Ono and Moslehi also fails to anticipate Applicants' invention or make Applicants' invention obvious.

Moslehi discloses a low-temperature, microwave-driven, plasma nitridation system which Applicant does not use or disclose. Applicants' nitridation method is a high-pressure gas and laser energy deposition approach. (Applicant page 6, lines 14-24). Applicants do not disclose a plasma or microwaves. Applicants disclose trimming films with a thickness up to 100 nm. (Application, page 15, line 4). Moslehi's invention produces a maximum thickness of 100 Angstroms (10 nm) (Moslehi, column 2, lines 47-50). Moslehi's invention is inadequate for Applicants' purposes.

not recited

The eximer laser method referred to as inferior prior art by and discarded by Moslehi was able to provide films only 25 Angstroms (2.5 nanometers) thick. (Moslehi, column 2, lines 9-13; lines) The minimum thickness Applicants disclose for a trimming film is 10 nanometers. (Application, page 15, line 3). The laser disclosed by Moslehi was a 15 mJ/pulse cm^2, 193 nm wavelength, ArF eximer laser which did not contribute significant

not recited

thermal effect to the process. The laser photochemically generated NH_2 radicals which enhanced nitridation. (See Exhibit 1, the article abstract from the AIP website,). This teaches away from laser heating the polysilicon gate. Applicants disclose the use of a high-power (400-500 mJ/pulse cm^2), 308 nm wavelength laser which melts the surface of the polysilicon gate. (Application, page 15, lines 13-15; page 14, lines 16-19) Thus, the cited eximer laser is not a useful part of Applicants' invention and could not be combined with anyone's teachings to form Applicants' invention.

In summary, none of the references cited by the Examiner nor any other known prior art, either alone or in combination, disclose the unique combination of features disclosed in applicant's claims presently on file. For this reason, allowance of all of Applicants' claims is respectfully solicited.

It is therefore submitted that the application defines patentable subject matter. Therefore, Applicants' claims currently on file are in condition for allowance. Such allowance at an early date is respectfully requested.

Accordingly, it is respectfully requested that the subject claims be reconsidered and allowed.

The Examiner is invited to telephone the undersigned if this would in any way advance the prosecution of this case.

Applicants hereby declare that any amendments herein are made for purposes of clarification, and that no such changes shall be construed as limiting the scope of the claims or the application of the Doctrine of Equivalents.

The Applicants herewith petitions the Commissioner of Patents and Trademarks to extend the time for reply to the office action dated June 6, 2001 for one (1) month. Enclosed is a firm check in the amount of $110.00 to cover the cost of the extension of time. Please charge IBM Corp. Deposit Account No. 09-0456 any additional fees, including additional extension of time fees, are due as a result of this response, please charge the above numbered deposit account. This authorization is intended to act as a constructive petition for an additional extension of time, should an additional extension of time be needed as a result of this response. Please credit any overpayment to the above numbered deposit account.

Respectfully submitted,

Date: October 9, 2001

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VIEW OF AMENDED PARAGRAPH SHOWING CHANGES

Paragraph Beginning at Line 20 of Page 10

FIG. 8 shows wafer portion 1300 wherein the order of the steps in method 100 has been changed such that step 120 follows step 140. That is, gate conductor 1340 has been trimmed by selective surface nitridation or oxidation (steps 122 or 124) with masking of gate conductor [1345] <u>1375</u> (step 129) after forming spacers and doping the source, drain, and gate. Accordingly, wafer portion 1300 includes gate conductor spacers 1250, which may be formed in step 120, 130, or both, and diffusion areas 1220. Wafer portion 1300 also includes a dielectric film 1360 grown on gate conductor 1340 after step 140 according to an alternative preferred embodiment of the present invention. As a further alternative, wafer portion 1300 would also be formed if gate conductor 1340 was doped, spacers 1250 formed, dielectric film 1360 grown, and then diffusion areas 1220 doped, but that option is not preferred since two doping steps are required. Dashed line 1325 indicates the dimension of the gate conductor prior to growth of dielectric film 1360 and shows that the dimension of gate conductor 1340 is reduced compared to its prior dimension. Also, FIG. 8 shows that dielectric film 1360 essentially forms a cap to isolate gate conductor 1340. In keeping with step 120, dielectric film 1360 may be removed or left in place. If left in place, then dielectric film 1360 may be useful in later forming borderless diffusion contacts as indicated in the copending patent application referenced above.

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Excimer laser enhanced nitridation of silicon substrates

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Abstract

Silicon direct nitridation has been successfully done using purified ammonia gas and an ArF excimer laser (lambda =193 nm). Direct nitride films were grown at a substrate temperature of 400 °C and a laser pulse energy of 15 mJ/pulse cm^2. As far as Auger signal intensities are concerned, there is little difference between the excimer laser enhanced nitrided films grown at 400 °C and thermally nitrided films grown at 1000 °C. The maximum film thickness grown is limited to 2.5 nm at 400 °C by diffusion of nitridation species across the grown film. The temperature rise on the substrate surface irradiated by the laser was calculated and found to be around 50 °C. Therefore, the thermal effect of the laser irradiation is of little significance in this experiment. The photochemically dissociated products of ammonia molecules were investigated by a quadrupole mass analyzer. The photochemically generated NH_2 radicals seem to enhance the nitridation.

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EXHIBIT 1